In the Claims

Claim 1 (previously presented): A method of forming a transistor gate, comprising:

forming a conductive material over a semiconductor substrate;

forming a block over and physically against the conductive material; the block consisting of photoresist and a single material other than photoresist which is against the photoresist; and

transferring a pattern from the block to the conductive material to pattern a transistor gate construction comprising the conductive material.

Claim 2 (original): The method of claim 1 further comprising removing the block from over the transistor gate construction.

Claim 3 (original): The method of claim 1 further comprising defining a channel region within the semiconductor substrate beneath the transistor gate construction; and forming source/drain regions within the semiconductor substrate and spaced from one another by the channel region.

Claim 4 (original): The method of claim 1 wherein the photoresist releases an acid, and wherein the material other than photoresist is a coating which cross-links when exposed to the acid from the photoresist.

Claim 5 (cancelled).

Claim 6 (cancelled).

Claim 7 (previously presented) A method of forming a transistor gate, comprising:

forming one or more conductive materials over a semiconductor substrate;

providing a photoresist block which is over a first portion of the one or more conductive materials and not over a second portion of the one or more conductive materials;

forming a layer over the photoresist block and over at least some of the second portion of the one or more conductive materials, the layer having a first segment that is against the photoresist block and a second segment that is not against the photoresist block;

treating the layer so that the first segment becomes different than the second segment;

after the treating, selectively removing the second segment of the layer while leaving the first segment of the layer; the photoresist block and remaining first segment together defining a masking block that is laterally wider than the photoresist block; and

transferring a pattern from the masking block to the one or more conductive materials to pattern a transistor gate construction from the one or more conductive materials.

Claim 8 (original): The method of claim 7 further comprising removing the masking block from over the transistor gate construction.

Claim 9 (original): The method of claim 7 further comprising defining a channel region within the semiconductor substrate beneath the transistor gate construction; and forming source/drain regions within the semiconductor substrate and spaced from one another by the channel region.

Claim 10 (currently amended): The method of claim 7 wherein the treatment includes causing the photoresist to release an acid which forms cross-links within the first segment of the layer.

Claim 11 (cancelled).

Claim 12 (previously presented): A method of forming a programmable read-only memory construction, comprising:

forming a conductive material over a semiconductor substrate;

forming a block over the conductive material; the block consisting of a photoresist mass and a single material other than photoresist which is against the photoresist;

transferring a pattern from the block to the conductive material to pattern a floating gate construction comprising the conductive material;

forming a dielectric material over the floating gate construction; and

forming a control gate over the dielectric material.

Claim 13 (original): The method of claim 12 further comprising defining a channel region within the semiconductor substrate beneath the floating gate construction; and forming source/drain regions within the semiconductor substrate and spaced from one another by the channel region.

Claim 14 (cancelled).

Claim 15 (original) The method of claim 12 wherein the photoresist releases an acid, and wherein the material other than photoresist is a coating which cross-links when exposed to the acid from the photoresist.

Claim 16 (cancelled).

Claim 17 (original): The method of claim 12 wherein the control gate, dielectric material and floating gate are incorporated into a FLASH memory device.

Claim 18 (currently amended): A method of forming at least two programmable read-only memory constructions, comprising:

forming at least one conductive material over a semiconductor substrate;

forming at least two patterned photoresist blocks over the conductive material; a pair of adjacent photoresist blocks being separated by a first gap;

forming a layer on the pair of adjacent photoresist blocks and across the first gap between the adjacent blocks, the layer having segments that are against the photoresist blocks and at least one segment that is not against the photoresist blocks, the at least one segment that is not against the photoresist blocks including a region of the layer that extends across the first gap, the segments that are against the photoresist blocks including regions of the layer that are on the pair of adjacent photoresist blocks;

treating the layer so that the segments that are against the photoresist blocks become different than the at least one segment that is not against the photoresist blocks;

after the treating, selectively removing the region of the layer from across the first gap while leaving the layer on the pair of adjacent photoresist blocks; the pair of photoresist blocks and layer remaining thereon together defining a pair of masking blocks that are separated by a second gap; the second gap being narrower than the first gap;

transferring a pattern from the masking blocks to the conductive material to pattern a pair of spaced floating gate constructions from the conductive material;

forming a dielectric material over the spaced floating gate constructions; and

forming control gate material over the dielectric material.

Claim 19 (previously presented): The method of claim 18 wherein the treating includes causing the photoresist to release an acid which forms cross-links within the layer.

Claim 20 (cancelled).

Claim 21 (original): The method of claim 18 wherein the control gate material, dielectric material and floating gates are incorporated into a pair of FLASH memory devices.

Claim 22 (original): The method of claim 18 wherein the patterned photoresist blocks are formed by a photolithographic process; wherein the photolithographic process is limited to a minimum feature size that can be obtained by the photolithographic process; and wherein a distance between the spaced floating gate constructions is less than said minimum feature size.

Claim 23 (original): The method of claim 22 wherein the first gap corresponds to about said minimum feature size.